LOW TEMPERATURE DIGITAL SUPERCONDUCTING ELECTRONICS

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13. ABSTRACT *(Maximum 200 words)*

Our aim was to further the development of low temperature superconducting digital electronics, to the point where real-world applications of this technology were practical. We concentrated on RSFQ (Rapid Single Flux Quantum) logic which should be capable of VLSI circuit operation at 100 Gbps with power of 100 nW per gate, if a semiconductor-quality fabrication facility were available. We developed the infrastructure for RSFQ circuits including the first logic-level simulator; the first industrial CAD environment; the first yield optimization; the first analysis of timing; the first HDL description. All software tools are available at our widely referenced web site. Our work continually emphasized the central importance of timing considerations for the design of RSFQ circuits, and we present many important results in this area. We developed the theory and performed the definitive experiments at 10 Gbps to understand the bit-error-rate of RSFQ circuits. Complex demonstration circuits were designed and demonstrated to work at speeds up to 20 Gbps. Finally, we developed a cryogenic electro-optic sampler which is a microvolt, subpicosecond, micron-scale, contact-free, fully-automated system, and used this to perform the direct first observation of an SFQ pulse as well as a variety of other studies.

14. SUBJECT TERMS

superconductivity; superconducting digital electronics; single flux quantum; RSFQ logic; SFQ pulses; decimation digital filter; timing; circular shift register; femtosecond pulses; MSM diodes; electro-optic sampling; crosstalk; residue number system; bit-error-rate

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A. Statement of the **PROBLEM** studied:

Our aim in this research was to further the development of low temperature superconducting digital electronics, to the point where practical real-world applications of this technology could be considered. We concentrated on the "Rapid Single Flux Quantum" (RSFQ) logic family. Our efforts were to develop the design-tool infrastructure necessary to realize significant RSFQ circuits; to develop the concepts and methodologies to advance this field; to design, have fabricated, and test real demonstration circuits to validate and to find the weaknesses of these design tools, concepts, and methodologies (our proposal promised a real time digital filter); and finally to develop techniques to characterize these ultra-high-speed circuits by subpicosecond electro-optic measurements of individual SFQ pulses.

B. Summary of the most important **RESULTS** (footnote numbers refer to publication list, next section):

Infrastructure: Design tools are necessary for the development of integrated circuits in any technology. We found the design infrastructure for RSFQ circuits sorely lacking, and much of our research was directed towards correcting this. Some of our innovations are the following: the first logic-level simulation of RSFQ circuits [3]; the first industrial CAD environment for RSFQ [50]; the first "optimization for yield" for RSFQ gates [31]; the first analytical investigation of RSFQ timing [30]; the first HDL description of RSFQ gates [48]. All of these new directions were quickly borrowed or emulated by other research groups, so quickly in fact that our publications were not always the first.

RSFQ circuit optimization is essential because of variations in the fabrication technology of superconducting devices. Optimization is slow and tedious, and previous techniques could give a poor choice for parameter values, which can cause circuit failure. We developed an optimization tool called MALT [31], using the method of inscribed hyperspheres to maximize yield rather than "critical margin." It optimizes a circuit with eight simultaneous variables in 1 - 2 hours. Many circuits redesigned using MALT have record simulated margins. MALT (and a users' guide) are available for distribution, and has rapidly become the standard throughout the research community.

We developed a simulation package for extraction of inductances in superconducting circuits [44]. (Inductor design is a crucial problem for superconducting circuits.) This appears to be superior to inductance extractors used by other research groups, probably because it is based on a true 3-D finite element program, the public-domain "FastHenry" developed at MIT.

These and all of the other tools developed in our group are available to the public. They are all collected on the group web site (http://www.ece.rochester.edu/~sde/). The web site also contains a description, analysis, and comparison of all the design tools used by all the other groups in the world. This web site is now universally acknowledged and widely referenced as the primary repository resource for RSFQ design tools; many groups have downloaded Rochester tools from this site.

Concepts and methodologies: In this area we concentrated on the timing/clocking of RSFQ circuits, built-in self test structures and techniques, and the bit-error rate of these circuits.

We have continually emphasized the central importance of timing considerations for the design of RSFQ circuits. This is similar to semiconductor circuits, but different in that the natural timing schemes for RSFQ logic have built-in clock skew [42]. We developed and analyzed several new clocking schemes for RSFQ [30,42,55]. For instance, we invented, developed, and analyzed a new 2-phase clocking scheme [55]. The maximum speed of RSFQ circuits is limited by fabrication-induced parameter variations. For most previous circuits this problem will grow with the size of the circuit -- large circuits will be slower than smaller circuits. Our 2-phase clocking avoids this problem with very little added overhead.

We performed a full timing analysis of a 4-bit RSFQ decimation digital filter design. This required an analysis of the timing requirements of each filter subcell, a careful assessment of current superconductor foundry technology to gauge the effects of fabrication-induced parameter variations on cell timing, and consideration of various clock distribution schemes. The optimized filter design simulates to 11 GHz with conservative counter-flow clocking and to 29 GHz with concurrent clocking. Fabrication-induced parameter variations reduce these numbers to 9 GHz and 14 GHz respectively, for 3-sigma reliability. This analysis suggests directions towards a more aggressive filter design, and we guess that a second generation filter design, using current fabrication technology, will operate above 30 GHz. If the resources existed to fabricate RSFQ circuits in semiconductor-quality facilities we would estimate that the filter design could operate at a clock rate of greater than 200 GHz [30,51].

These are only a few of the topics we have covered which relate to the timing of RSFQ circuits. Some other important results can be found in [30,49,64,65,66].

Output from RSFQ circuits can be difficult, both because of the high-speed beyond that of laboratory instruments, and because of the small energy of the SFQ pulse. We developed a number of built-in self test structures and techniques in order to perform high speed experiments without high speed output [47], and have since successfully used these to perform the experiments described below.

We performed what is still the definitive SFQ error-rate experiment, based on XOR-ing the outputs of two nominally identical digital circuits operating at 10 GHz [37]. The frequency of bit errors could be varied over a wide range by adjusting the bias current from optimal to approach the failure point. In this way we measured the BER over 16 decades of incidence. A linear extrapolation gave a minimum error rate of order 10^{-50} per bit operation. To acquire the lowest data point required 4 errors counted in 130 hours at a 10 GHz clock rate. The entire experiment lasted for nine days. For various reasons the experiment was repeatedly stopped and restarted and data taken different ways. Yet, in spite of these "disruptions," the operation of the circuit and the error rate were perfectly stable during the entire experiment. We also performed the same experiment while the chip was in an applied magnetic field, which gives insight into an important issue for large RSFQ circuits -- flux trapping. We saw no new error mechanisms due to trapped flux.

We developed a theory to predict the bit-error-rate of RSFQ circuits based on the Fokker-Planck equation [46], assuming that all errors are instigated by thermal noise from the circuit resistors at some effective temperature T^*. No other such theory exists. We compared the theory to the experiment and found excellent agreement, with $T^* = 11$ K rather than the physical temperature 4.2 K. A similar experiment was performed as a function of temperature [63] showed that this factor of ~2 is real, but that the errors are indeed of thermal origin. The theory predicts that a high-T_c digital circuit operating at 77 K would not be useful.

<u>Demonstration circuits</u>: Our first very early design for a 4-bit RSFQ decimation digital filter [3] was perhaps the most complicated circuit that had ever been designed specifically for RSFQ logic. The eventual design that was actually realized [45] was changed in only minor ways. Every component was successfully tested at low speed. The most complex unit of the filter is the multiplier-accumulator, which contains 1100 Josephson junctions. It works perfectly at low speed, with full functionality and stable operation over the 24 hour testing period. It may be surprising to note that this is arguably the most complex RSFQ circuit ever verified experimentally. Most successful RSFQ circuits have been quite small, containing only tens or perhaps hundreds of junctions, or have been simple repetitive structures. The most difficult aspect required careful attention paid to clock distribution and timing in our design procedures.

The high-speed verification of the filter at 10 GHz using the built-in self test structures mentioned above has not succeeded, through several generations of design. In each case we discovered specific errors which suggested improvements to our design tools, and which were corrected in the next generation. Eventually this effort was suspended because of the graduation of several graduate students and because of other priorities.

Among other experimental accomplishments is an RSFQ 64-bit circular shift register (CSR) successfully operated at clock frequencies up to 18.5 GHz [61]. This is by far the longest recurrent data path, and by far the highest frequency, ever demonstrated in a *recurrent* RSFQ circuit. Data was circulated around all 64 stages about 50 million times before its integrity was verified. We also determined the various failure modes for over- and under-

biased clock and data lines, as a function of frequency [65]. The maximum *theoretical* operating frequency for this particular circuit was 21 GHz -- that close an agreement between theory and experiment is unprecedented in this immature field, and shows our good understanding of the issues involved.

We designed a one decimal-digit adder which is based on the residue number system (RNS) rather than binary arithmetic [28]. The most complex part of this adder, which is the mod5 adder, was completely verified at low speed [57,70]. A design flaw prevented the entire mod5 adder from working at high speed, but part of it at least was operated up to 20 GHz (the highest speed available from this particular on-chip clock) with excellent margins, suggesting a much higher maximum frequency.

Electro-optic research: We constructed a dedicated Cryogenic Electro-Optic Sampling Laboratory. The E-O sampler is a microvolt, femtosecond, micron-scale, contact-free, fully-automated system [7,27].

We developed two unique methods to generate SFQ pulses (traditional techniques to generate picosecond pulses require special substrates, derivative circuits, etc.). The first uses pulse excitation of a metal-semiconductor-metal photodiode. We have demonstrated this technique using both GaAs [1,2] and Si [5,6,13] diodes, and developed theories to understand fully the mechanisms involved. The Si-based MSM diodes were fabricated with standard superconductor foundry processes and were successfully tested for cryogenic E-O sampling. The second technique, "edge illumination" of a metal-semiconductor interface, allows even easier fabrication [12,22,32]. Again, the technique was investigated theoretically as well as experimentally [23]. A third technique is direct light excitation of a Josephson junction. These three techniques can also be used for optical input, or clocking, for superconducting circuits.

We performed the first observation of an SFQ pulse [20,25]. This accomplishment is analogous to the first observation of atoms with the advent of the STM. The experiment employed an optically triggered Nb-Si-Nb MSM diode to drive a "pulse-shaper" consisting of a 2-junction JTL with 100 μm separation. The SFQ pulse was mapped out in ten minutes sampling by measuring the optical polarization shift caused by the fringe field of the superconducting microstrip. The experiment was unambiguous. The pulse height was typically 0.7 mV with a pulse width of 3 ps, while the rms noise of the measurement was less than 70 μV and the time resolution was 0.2 ps. The integrated voltage was 2.0 ± 0.2 mV·ps, as required by theory, which establishes that the calibration procedures are absolutely correct.

We performed a variety of other studies. For instance we measured the crosstalk of overlapping microstrips and found that in some instances crosstalk could contribute to bit errors [60,67]. We experimentally verified that closely spaced SFQ pulses repel each other when traveling on a Josephson transmission line [68], an effect which could destroy circuit timing if care were not taken. We built an interferometric subpicosecond imaging system as well, which can measure voltages over a large area of the chip [38,39].

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D. All participating scientific **personnel**, advanced degrees earned while employed this project.

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5. Report of **INVENTIONS**: No reportable inventions